# Edge Testbed Demo

## Open Hardware Initiative – Intern Research Project

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Project Outline: Implement a binary classifier in the Edge Testbed

1. In python, train an SVM binary classifier to determine if object is an apple or not

    a. Fruits 360 dataset

2. Implement the SVM onto the testbed

    a. Port from python to c code

3. Use the Arducam camera module (OV2640) to input images into the testbed

4. Extract features from images

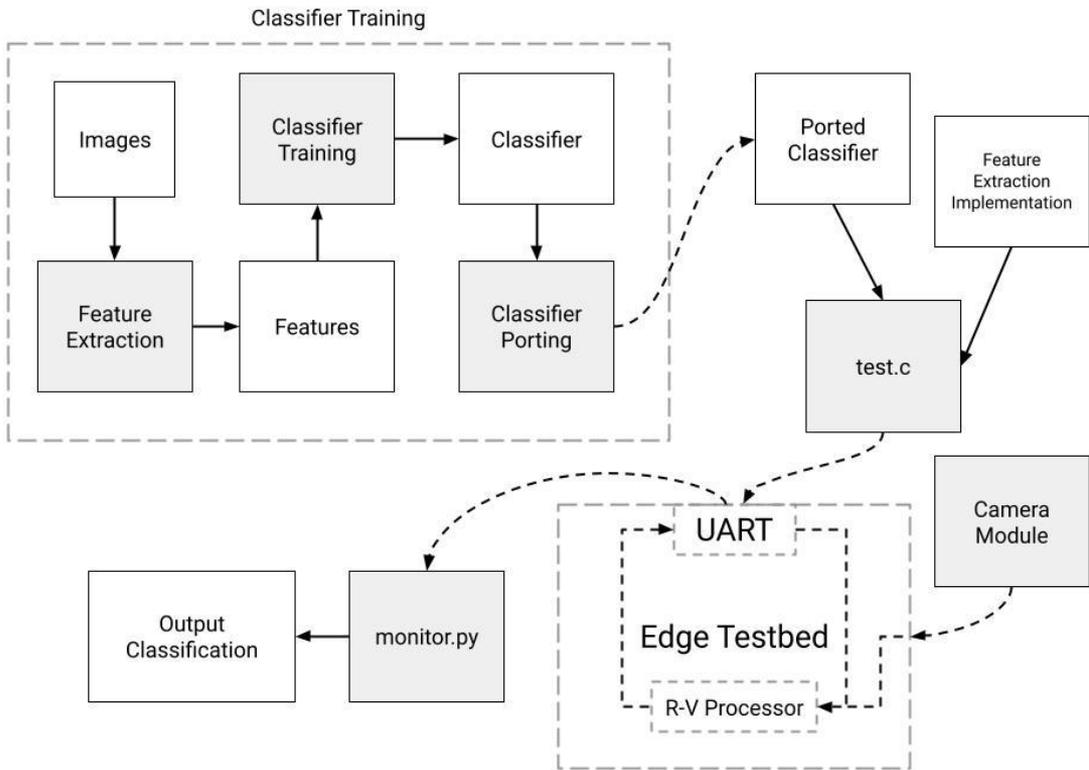5. Pass features into SVM classifier
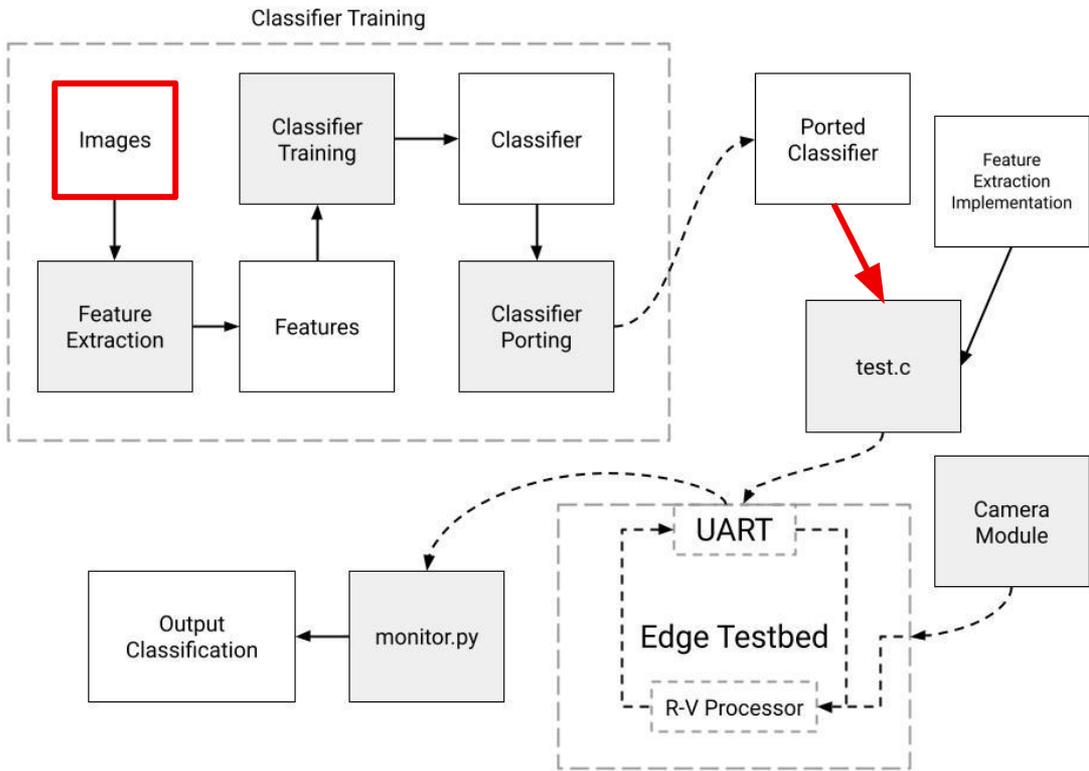
6. Output classification

Edge Testbed Flow
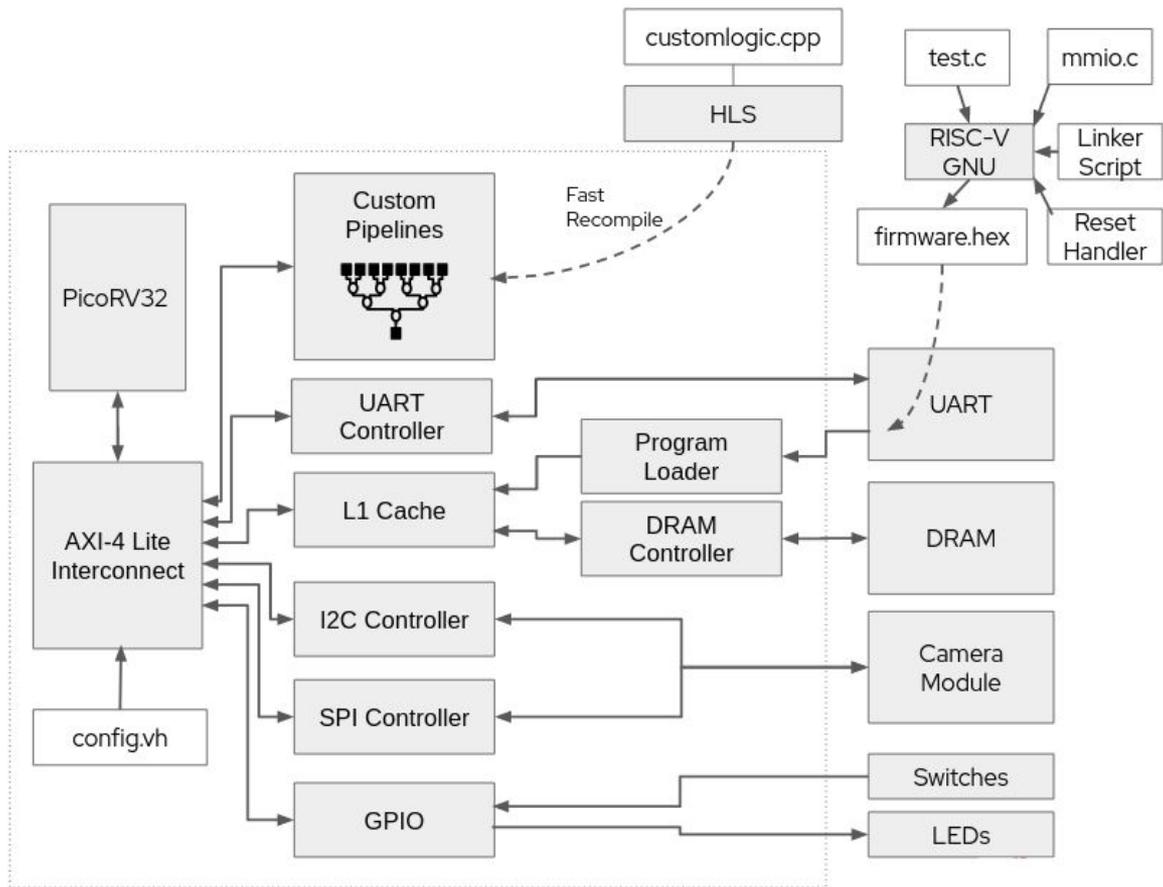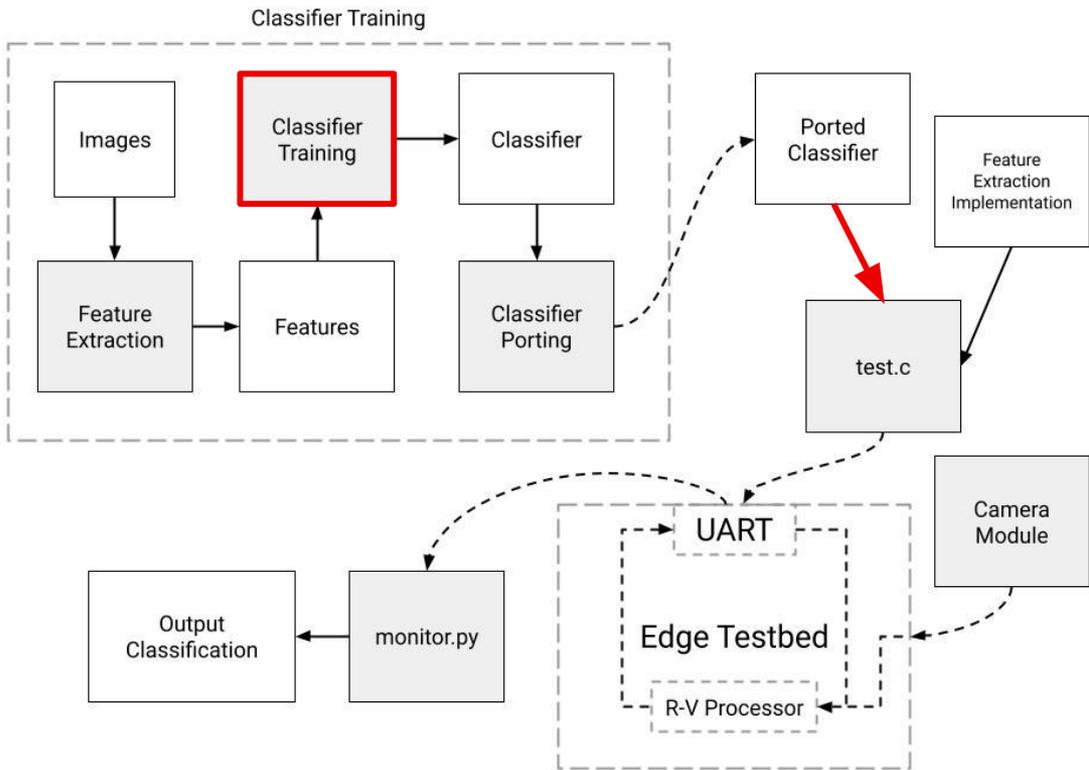
Classifier Implementation Flow
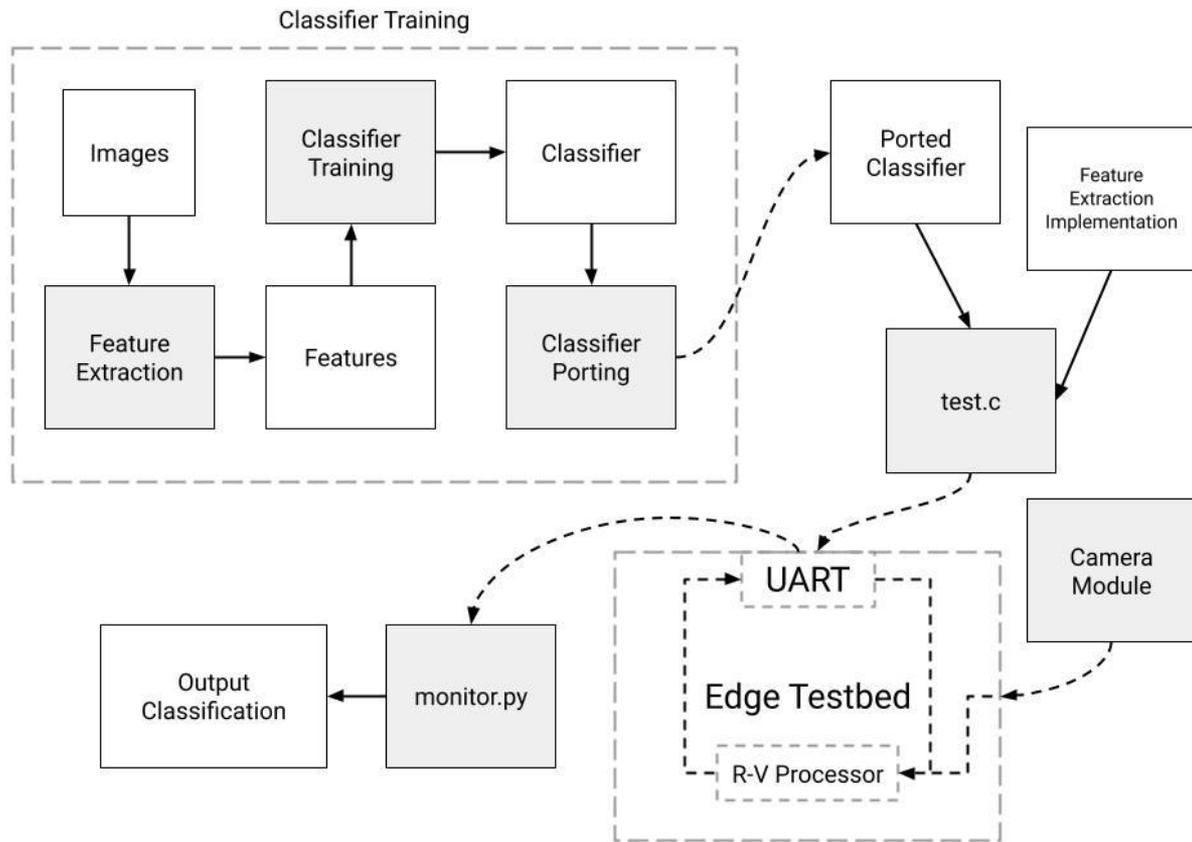
- Established workflow
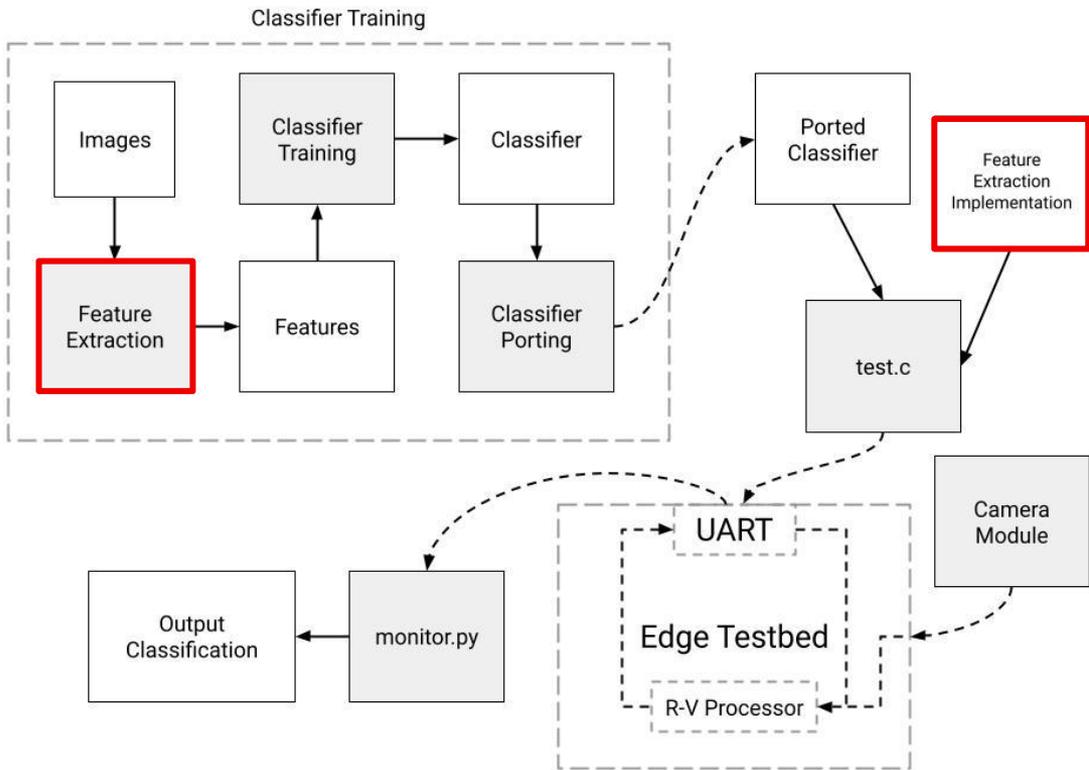 - Extremely easy to modify any portion of the classifier and reimplement

- Changing the training images

- Hyperparameter tuning

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- Changing the type of feature extraction

Why does this matter?

- Versatility of hardware
  - Much easier to modify
    - Just reload the program
- Encourage development for the testbed
  - Currently reliant on Xilinx tooling; Intel FPGA wouldn't work
    - Ideal environment works in any hardware environment

- Resolve vendor lock-in
  - Compatible with any hardware
    - Put together your own device, low cost
  - Utilize products from any vendor side-by-side
  - Creating alternatives
    - Lack of alternatives is a common reason for lock-in

Our Process

- Learning the tooling
  - Xilinx (Vivado and Vitis HLS)
  - Updating existing testbed frame code to avoid deprecated functions/packages
- Resolving OS differences
  - Some packages didn't exist on RHEL vs Fedora vs Ubuntu
  - Package versions weren't the same
- Simulation
  - Before actually implementing the physical board, we simulated the workflow just on local machines
- Moving to hardware

Challenges

- Open-source documentation isn't always perfect
  - *micromlgen* – python classifier porter
    - Documentation listed a porter to C but only ported to C++
- Choose a feature extractor then decided unviable
  - Raw -> SURF -> ORB -> HOG -> Color Average
- Binary classification vs multiclass classification
  - Originally implemented 'binary' classifier for apple v. orange
- Risc-V build limitations
  - Current R-V processor doesn't support float operations
  - Needed to emulate these operations

Thanks!

Check out the repo or send me a question!

 https://github.com/asanaullah/edge_testbed

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